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1. **EASTMAN KODAK: Kodak to distribute FotoWire Internet Photo Printing in connection with retail digital mini-labs; FotoWire solution enables photofinishers to accept digital prints orders online**
M2 Presswire. Coventry: Sep 15, 2000. p. 1
Full text Abstract

2. **Eastman Kodak to Launch Photo-CD Product**
By Alec Klein. **Wall Street Journal (Europe).** Brussels: Feb 9, 1999. p. 8
Full text Abstract

3. **Kodak Designs Spectrum Signal Processing's DSP-Based Detroit Product Into New Digital Lab System; Kodak Recognizes Spectrum as an ISO 9001 Certified Supplier**
Business Editors. **Business Wire.** New York: Dec 1, 1998. p. 1
Full text Abstract

4. **Eastman Kodak and Intel Join Forces To Offer Photographs on Compact Disk**
By Laura Johannes and Alec Klein. **Wall Street Journal (Eastern edition).** New York, N.Y.: Sep 28, 1998. p. 1
Full text Abstract

5. **EASTMAN KODAK: Kodak demonstrates leadership across entire photographic category**
M2 Presswire. Coventry: Feb 13, 1998. p. 1
Full text Abstract

6. **THE GIMMICK THAT WILL NOT DIE; [THIRD Edition]**
Nathan Cobb, Globe Staff. **Boston Globe (pre-1997 Fulltext).** Boston, Mass.: Apr 8, 1988. p. 45
Full text Abstract

1-6 of 6

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1. **Philips to Produce Devices For Looking at Kodak CD's**
New York Times (Late Edition (East Coast)). New York, N.Y.: Aug 25, 2001. p. C.3
Full text | Abstract

2. **Digital Developments**
Greg Masters. **Retail Merchandiser.** New York: Feb 2001. Vol. 41, Iss. 2; p. 43 (3 pages)
Text+Graphics | Page Image - PDF | Abstract

3. **EASTMAN KODAK: Kodak to distribute FotoWire Internet Photo Printing in connection with retail digital mini-labs; FotoWire solution enables photofinishers to accept digital prints orders online**
M2 Presswire. Coventry: Sep 15, 2000. p. 1
Full text | Abstract

4. **Eastman Kodak to Launch Photo-CD Product**
By Alec Klein. **Wall Street Journal (Europe).** Brussels: Feb 9, 1999. p. 8
Full text | Abstract

5. **Kodak Designs Spectrum Signal Processing's DSP-Based Detroit Product Into New Digital Lab System; Kodak Recognizes Spectrum as an ISO 9001 Certified Supplier**
Business Editors. **Business Wire.** New York: Dec 1, 1998. p. 1
Full text | Abstract

6. **Eastman Kodak and Intel Join Forces To Offer Photographs on Compact Disk**
By Laura Johannes and Alec Klein. **Wall Street Journal (Eastern edition).** New York, N.Y.: Sep 28, 1998. p. 1
Full text | Abstract

7. **Put yourself in the digital picture Cutting, pasting and darkroom work can be done on your computer; [All Edition]**
DOUGLAS D. ARMSTRONG. **Milwaukee Journal Sentinel.** Milwaukee, Wis.: Feb 16, 1998. p. 9

Full text Abstract

8. **EASTMAN KODAK: Kodak demonstrates leadership across entire photographic category**
M2 Presswire. Coventry: Feb 13, 1998. p. 1

Full text Abstract

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Petersen's Photographic; Los Angeles

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File 474:New York Times Abs 1969-2005/Sep 18
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File 99:Wilson Appl. Sci & Tech Abs 1983-2005/Jul
(c) 2005 The HW Wilson Co.
File 348:EUROPEAN PATENTS 1978-2005/Sep W02
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File 349:PCT FULLTEXT 1979-2005/UB=20050915,UT=20050908
(c) 2005 WIPO/Univentio
File 347:JAPIO Nov 1976-2005/Apr(Updated 050801)
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Set     Items   Description
S1     148054   (STORE OR RETAILER OR SHOP) (10N) ((COMPUTER? OR
(IMAG?????
               (5N) (DEVICE OR KIOSK))))
S2       3455   (TRANSFER? (10N) (IMAGE OR PICTURE) (5N) (MEDIA OR DISK
OR
             FLOPPY))
S3         19   S1 (S) S2
S4         14   S3 AND PY<2002
S5         14   RD S4 (unique items)
S6          5   S5 AND (ORDER OR TRANSACTION)
?



? t s6/3,k/1-5

 6/3,K/1     (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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01189094
Printer and printer data processing method
Drucker und Verfahren zur Bearbeitung von Drucker-Daten
Imprimante et methode de traitement de donnees d'Imprimante
PATENT ASSIGNEE:
  SEIKO EPSON CORPORATION, (730004), 4-1, Nishishinjuku 2-chome,
    Shinjuku-ku, Tokyo 163-0811, (JP), (Applicant designated States:
all)
INVENTOR:
  Shima, Toshihiro, c/o Seiko Epson Corp., 305 Owa 3-chome, Suwa-shi,
    Nagano 392-8502, (JP)
LEGAL REPRESENTATIVE:
  Sturt, Clifford Mark et al (50502), Miller Sturt Kenyon 9 John Street,
    London WC1N 2ES, (GB)
PATENT (CC, No, Kind, Date):  EP 1035467  A2  000913 (Basic)
                              EP 1035467  A3  020508
APPLICATION (CC, No, Date):   EP 2000301857 000307;
PRIORITY (CC, No, Date): JP 9962962 990311
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT;
LI;
  LU; MC; NL; PT; SE
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: G06F-003/12
ABSTRACT WORD COUNT: 134
NOTE:
  Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text  Language   Update    Word Count
      CLAIMS A  (English)  200037     1839
      SPEC A    (English)  200037     5625
Total word count - document A         7464
Total word count - document B            0
Total word count - documents A + B    7464
```

...SPECIFICATION is recently proposed.
As a printer in which the above auxiliary storage is built can **store**
a large quantity of data, it can release a host **computer** early.
However, in the auxiliary storage, as a head is moved to a predetermined
position...

...received from a network is 1 to 2 MB/s. and the processing of an **image**
data generator is 1 MB/s., the data **transfer** rate of a hard **disk**
drive (HDD) is normally approximately 500 kB/s. and is slow.
Therefore, when print job...

...selected in case data being processed is not stored in the auxiliary storage.
As the **order** of printing and others are disordered when data is
transferred to the image data generator...auxiliary storage as shown in
Fig. 12C.
Besides, processing may be also executed in the **order** of the first
bypass mode, the second bypass mode, the mode via the auxiliary storage
...

...the second bypass mode and printing is terminated). Processing may be
also executed in the **order** of the first bypass mode, the mode via the
auxiliary storage, the second bypass mode...

...case a file remaining in HDD 10 exists, processing speed can be
enhanced, preventing printing **order** from being disordered.
Fourth, as not only the first bypass mode from the communication task
...

6/3,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00917928
An image forming apparatus using an intermediate transfer belt and a method
for the same
Bilderzeugungsvorrichtung unter Verwendung eines Zwischenubertragerbandes
und Verfahren dazu
Appareil de formation d'images utilisant une bande de transfert
intermediaire et methode pour ceci
PATENT ASSIGNEE:
Ricoh Company, Ltd., (209036), 3-6, Nakamagome 1-chome, Ohta-ku, Tokyo 143, (JP), (Proprietor designated states: all)
INVENTOR:
Yanagawa, Nobuyuki, 4-15-60, Nakakaigon, Chigasaki-shi, Kanagawa, (JP)
LEGAL REPRESENTATIVE:

Schwabe, Hans-Georg, Dipl.-Ing. (10921), Patentanwalte Schwabe, Sandmair,
Marx Stuntzstrasse 16, 81677 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 837373 A1 980422 (Basic)
EP 837373 B1 030319
APPLICATION (CC, No, Date): EP 97117953 971016;
PRIORITY (CC, No, Date): JP 96273350 961016; JP 96313654 961125; JP 97261753 970926
DESIGNATED STATES: DE; FR; GB; IT; NL
RELATED DIVISIONAL NUMBER(S) - PN (AN):
EP 1202126 (EP 2002002050)
(EP 2003002017)
INTERNATIONAL PATENT CLASS: G03G-015/01
ABSTRACT WORD COUNT: 12173
NOTE:
Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200312	1842
CLAIMS B	(German)	200312	1639
CLAIMS B	(French)	200312	2115
SPEC B	(English)	200312	5359
Total word count - document A			0
Total word count - document B			10955
Total word count - documents A + B			10955

...SPECIFICATION Visible images formed by both image forming means are transferred one over the other in **order** to improve the quality of the recorded image without lowering the processing speed. While this... full-color image is transferred to the second paper P2. This image transfer to the **paper** P2 occurs while the belt 66 in the fourth turn.

(6) The third printing is...B color toner image to the belt 66 over the preceding A color toner image **to** thereby form an A/B toner image.

At this instant, the belt 66 substantially completes...4 is identical in construction with the first image forming unit I and includes a **drum** 75-2, a writing device 77-2, a B color developing device 300, a D...

...developing device 100 and C color developing device 200 of the first developing unit I **store** magenta toner and cyan toner, respectively. The B color developing **device** 300 and D color **developing** **device** 400 of the second developing unit II positioned closer to an image transfer position 79...with the intermediary of the belt 66 so as to clean the surface of the **belt** 12.

A paper feed device, not **shown** , is located below **the** **image** **forming** units I and II in **order** to feed papers or **similar** **recording** **media** one by **one** **to** the right, as viewed in FIG. 4. A paper P fed from the sheet feed...

...heat roller 86. A roller 88 may be pressed against the heat roller 86 in
order to apply an anti-offset liquid to the roller 86.
An outlet roller pair 89...
...for discharging heat is located above and at the left of the tray 90 in
order to protect electronic parts positioned below the tray 90 from heat.
When L = 1 + (alpha...

...this requirement, the magnets of the other or inoperative three rollers
are slightly rotated in **order** to shift their poles with respect to the
drums. Alternatively, the inoperative developing rollers may...above and
at the right of the belt 66A, as viewed in FIG. 6, in **order** to remove
toner to remain on the belt 66A after image transfer.
The first image

...CLAIMS color developing means (100) and said C-color developing means
(200) are arranged in this **order** along said first image carrier
(75-1) in a direction of movement of said first...

...said black developing means (400) and said B-color developing means are
arranged in this **order** along said second image carrier (75-2) in a
direction of movement of said second...second image forming unit (II)
and said transferring means (68) are sequentially arranged in this
order in a direction of movement of said intermediate transfer belt
(66), and wherein the developing...
...second image forming unit (II) and said transferring means (68) are
sequentially arranged in this **order** in a direction of movement of
said intermediate transfer belt (66), and wherein the developing

6/3,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00486829
Compressed image stores for high resolution computer graphics
Komprimierten Bildspeicher fur hoch-auflosenden Rechnergraphik
Memoires d'image compressees pour graphiques haute-resolution par calculateur
PATENT ASSIGNEE:
CANON KABUSHIKI KAISHA, (542361), 30-2, 3-chome, Shimomaruko, Ohta-ku, Tokyo, (JP), (applicant designated states: DE;FR;GB;IT)
CANON INFORMATION SYSTEMS RESEARCH AUSTRALIA PTY LTD., (1389530), 1 Thomas Holt Drive, North Ryde, NSW 2113, (AU), (applicant designated

states: DE;FR;GB;IT)
INVENTOR:
Silverbrook, Kia, 40, Bathurst Street,, WOOLLAHRA, New South Wales 2025,
(AU)
LEGAL REPRESENTATIVE:
Beresford, Keith Denis Lewis et al (28273), BERESFORD & Co. 2-5 Warwick
Court High Holborn, London WC1R 5DJ, (GB)
PATENT (CC, No, Kind, Date): EP 473341 A2 920304 (Basic)
EP 473341 A3 930224
EP 473341 B1 970409
APPLICATION (CC, No, Date): EP 91307564 910815;
PRIORITY (CC, No, Date): AU 901784 900816; AU 901785 900816; AU 903418 901119
DESIGNATED STATES: DE; FR; GB; IT
INTERNATIONAL PATENT CLASS: G06T-009/00;
ABSTRACT WORD COUNT: 110

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPAB97	1042
CLAIMS B	(German)	EPAB97	925
CLAIMS B	(French)	EPAB97	1157
SPEC B	(English)	EPAB97	5011
Total word count - document A			0
Total word count - document B			8135
Total word count - documents A + B			8135

...SPECIFICATION the prior art system of Fig. 1B requires 96 MBytes of data
storage for each **image** within the data storage unit 12, which is generally a hard disk drive. Also, 96 MBytes of information must be **transferred** from the storage **device** 12 to the **image store** 6 for each image to be printed on the printer 15. Also, the computer 11 must calculate 32 million pixels, each with 24 bits of information, in **order**
to generate a single A3 image. The calculation of such images is inherently slow.
Suitable...5 is a schematic block diagram of a second preferred embodiment;
Fig. 6 illustrates the **order** in which the pixels of an A3 page are
printed;
Figs. 7A and 7B shows...57, and back through the compressor 58 via the
compositor 55. As a result, the **order** of the ADCT compressed image is
not upset by having to modify a particular portion...

...compositing step, 579 blocks of 8 X 8 pixels are expanded, composited and compressed. In **order** that expansion, compositing and compression can occur simultaneously, three buffers are provided, an expansion buffer
...ADCT compressed image requires that the image must always be calculated in essentially the same **order** as the printer requires the

output data for printing. The printing process used in the...

...them in a pixel mapped (or bit mapped for black and white) image store.
In **order** to create the image shown in Fig. 7A, the image is written object by object...
...each object must be created for each band. Accordingly, with reference
to Fig. 8, in **order** to create each band, the various objects are divided into bands and the respective bands...

...scan lines) in one pass. This rendering process must be repeated for 810
bands in **order** to render an entire A3 image.
Fig. 9 shows a graphics system 300 similar to...

6/3,K/4 (Item 4 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00430529
Fault tolerant data processing system initialisation
Initialisation eines fehlertoleranten Datenverarbeitungssystems
Initialisation d'un systeme de traitement de donnees a tolerance de fautes
PATENT ASSIGNEE:
International Business Machines Corporation, (200120), Old Orchard Road,
Armonk, N.Y. 10504, (US), (applicant designated states:
AT;BE;CH;DE;DK;ES;FR;GB;GR;IT;LI;LU;NL;SE)
INVENTOR:
Freeman, Bobby Joe, 1381 S.W. 28th Avenue, Boynton Beach, FL 33426, (US)
Dinwiddie, John Monroe, Jr., 112 Pacer Circle, West Palm Beach, FL 33414,
(US)
Grice, Lonnie Edward, 252 N.W. 44th Street, Boca Raton, FL 33431, (US)
Loffredo, John Mario, 2694 S.W. 14th Drive, Deerfield Beach, FL 33442,
(US)
Sanderson, Kenneth Russell, 1132 Widgeon Road, West Palm Beach, FL 33414,
(US)
Suarez, Gustavo Armando, 21482 Woodchuck Lane, Boca Raton, FL 33428, (US)
LEGAL REPRESENTATIVE:
Bailey, Geoffrey Alan (27921), IBM United Kingdom Limited Intellectual Property Department Hursley Park, Winchester Hampshire SO21 2JN, (GB)
PATENT (CC, No, Kind, Date): EP 405736 A2 910102 (Basic)
EP 405736 A3 940202
EP 405736 B1 971217
APPLICATION (CC, No, Date): EP 90305310 900516;
PRIORITY (CC, No, Date): US 353112 890517
DESIGNATED STATES: AT; BE; CH; DE; DK; ES; FR; GB; GR; IT; LI; LU; NL; SE
INTERNATIONAL PATENT CLASS: G06F-011/16; G06F-009/44; G06F-015/177;

ABSTRACT WORD COUNT: 219

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	9712W2	701
CLAIMS B	(German)	9712W2	620
CLAIMS B	(French)	9712W2	806
SPEC B	(English)	9712W2	71242
Total word count - document A			0
Total word count - document B			73369
Total word count - documents A + B			73369

...SPECIFICATION with said functions being indiscernible by the operating system of the resource managing system.

In **order** that the invention may be fully understood a preferred embodiment thereof will now be described...O channel or bus. Each architecture device has a communications controller to exchange data. In **order** to communicate, a multi-layered protocol must be utilized to allow data to be exchanged...to the programmer. It is only when we want to connect multiple systems together in **order** to share I/O devices and distribute processing that this 'image' seen by the programmer...

...even cables) forces the programmer to understand - and learn to handle - the dual environment, in **order** to take advantage of the expanded facilities.

Generally, in **order** to access facilities ...The unbound message queue 189 stores all messages received via the BCU 154 in chronological **order** . Each entry is 16 bytes long.

The read pointer (RPNTR) and write pointer (WPNTR) in...

...by the PE 85 with a control microinstruction. It advises BCU 156 to fetch an **order** from the mailbox 188 and to execute it. The request is reset by the BCU after execution of the **order** . The state of the request can be sensed by the PE 85.

The BCU 156 makes a request when a problem occurs either during execution of an **order** initiated by the PE 85 or at any other time. It causes an exception in...two bit buffers/registers in adapter 154 and BCU 156 and in which the higher **order** (left) and lower **order** (right) bits of the information are placed on the eighteen bit channel 0, 1 buses...

...154. The inbound message queue 189 stores all messages sent by the BCU in chronological **order** .

3. The Bus Control Unit 156 - General Description (Figs. 16, 17)
The Bus Control Unit...entries to be easily moved or inserted without having to reorganize the array into sequential **order** . Also, the number of entries in the array need not be specified to the DMAC...the processor 62, a unique address configuration is presented on the address bus 161A in **order** to identify the type of cycle and priority level being serviced. This is also effectively...The net effect is transparent pre-emption of the previously running (lower priority) program in **order** to execute the higher priority interrupt handler.
The DMAC 209 interrupts in the preferred embodiment...

...88 processor 62 applies a virtual address on address bus 161A, with the four high **order** hex digits equal to "007E" (implying decoupling of PE62 from its S/88 hardware and...a DMAC register.
The address bus 247 is selected by PE 62 when the high **order** digits decode to hexadecimal (H) 007E.
The remaining four hex digits provide the local storage...

...bbbb) the byte transfer count are set into the DMAC memory transfer counter:
26 = High **order** byte count bit (=1 for max byte count (4096 only)).
25-16 = Lower **order** byte count bits. Bits 26-16 represent 1/4 of actual byte count (db1 word...

...subsequent BSM Read/Write Select Up command;
31-27 = Ignored by the BCU
26 = High **order** byte count bit. This bit will equal 1 only when the maximum byte count is...

...mix) to register 220 or 222 adapter requires a count of 1111 1111 1111 in **order** to transfer 4096 bytes (byte count 1). Therefore, the BCU 156 will decrement the doubleword...

...offset bits 15-14 (in 64 byte blocks) to bus adapter 154.
15-14 = Low **order** byte count bits. These bits represent the byte offset minus 1 (for bus adapter requirements...from the S/88 processor 62 to the local storage 210 are as follows: low **order** bits 0,1 (and SIZ0, 1 of PE 62, not shown) determine the number and...

...In the link list mode, the DMAC address bit A2 is used as the low **order** address bit (double word boundary) to the local storage 210. Since the

DMAC 209 is a word oriented (16 bit) device (A1 is its low **order** address bit) and since the local storage 210 is accessed by doubleword (32 bits), some...

...by reading the same doubleword location in store 210 twice, using A2 as the low **order** address bit. Bit A1 is then used to select the high/low word from the...

...the local store read/write mode, the DMAC bit A1 is used as the low **order** address bit to the local storage 210. The read data is supplied to storage 210...

...Channel 1 write buffer 228. Since the DMAC is a 16 bit device, the low **order** address bit is intended to represent a word boundary. However, each DMAC operation accesses ...will cause address bits A14 - A01 to be presented to the local storage 210. In **order** to allow for correct operation, the DMAC is loaded with 1/4 of the actual...

...doubleword accesses. The UDS and LDS signals cause accessing of high (D31-D16) and low **order** portions (D15-D0) local store 210.

In the PE 62 to DMAC 209 mode, the...

...will write the DMAC registers in each of the four DMAC channels 0-3 in **order** to set up the internal controls for a DMAC operation. PE 62 also has the...

...32 bits. This allows the DMAC 209 to take as many cycles as necessary in **order** to perform the DMAC load properly.

The S/88 processor SIZ0, SIZ1 (not shown) and...

...LDS (Lower Data Strobe) inputs (not shown) to the DMAC 209. This is required in **order** to access byte wide registers in the DMAC 209 as described more fully in the...

...from the logical NOT of A0. The SIZ0 line is used to access the low **order** byte when a word wide register is being accessed (NOT SIZ0). The SIZ1 line is used to access the low- **order** byte when a word wide register is being accessed via a "three byte remaining" S...

...operation. There are other adapter bus restrictions that must be obeyed by the hardware in **order** to meet the protocol requirements. The following is a detailed description of the BCU 156...

...capability. Since all transfers are done on a doubleword basis, bit 2 is the low **order** decrement bit. The r and s bits are latched by the BCU and presented to...controller 153. They transfer data strings from 1-64

bytes in length in ascending address **order** . The 32 bit command format
includes a real byte address in the three low **order** bytes and the high
order byte includes a highest **order** bit "0", next highest **order** bit
defines a fetch or store operation and the remaining six bits define the
length...the Input-Ready (IR) control signal is high. The data is output
in the same **order** as it was stored under the control of the Shift-Out
(SO) input when the...are sent back and forth. There is a queue which
holds the messages in FIFO **order** for the receiver on each end. There is
also a notification mechanism (PU to BCU...what is called a pending
interrupt table or PIT. PIT entries are chained in FIFO **order** to the
DST entry representing the S/370 device causing the interrupt. Stacking
an interrupt...the Channel 1 adapter bus 251,252. The S/88 processor 62
initializes the high **order** words of DMAC Channel 1 and 2 memory address
registers to zero (0). This saves...

...address of local buffer in store 210 for the I/O write data. The high
order data bus bits (31-16) will be loaded into the low **order** (15-00)
part of the channel 1 memory address register. The high **order** bits
(31-16) of the MAR were set to O during initialization. The DMAC 209...

...in Fig. 4SF wherein the bit designation is as follows:
31-27 = Reserved
26 = High **order** byte count bit. This bit will = 1 only when the maximum
byte count (4K bytes...

...count operations below. The bus adapter 154 requires a count of 1111
1111 1111 in **order** to transfer 4096 bytes (byte count -1). Therefore,
the BCU 156 will decrement the double...

...bits 15-14 (in 64 byte blocks) to the bus adapter 154.
15-14 = Low **order** byte count bits BCU 156.

These bits represent the byte offset minus 1 (for bus...

...preceding byte(s) are discarded.
05-00 = Reserved.
The DMAC 209 will load the high **order** word (i.e., byte count) of the
data bus into the channel I MTC register...not on a doubleword boundary,
(bits 07-00 = 01001010), the following action takes place in **order** to
load the BCU 156 and the DMAC 209 with one S/88 processor command...

...The BCU logic 253 then raises TAG UP line 262a to bus adapter 154 in **order** to latch the command, field length data into adapter command register 124 (Fig. 13) and...

...a 'BUS REQ' on line 269 to the BCU local bus arbitration logic 216, in **order** to perform a local bus cycle.
When bus grant signal on line 268 is returned...

...present a new BSM starting address to bus adapter 154 via registers 231, 219 in **order** to fetch the next 64 bytes. The register 231 has been decremented for each four...16 = starting address of local buffer I/O read data
15-00 = Reserved.
The high **order** data bus bits 31-16 will be loaded into the low **order** (15-00) bits of the Channel 2 memory address register. The high **order** bits (31-16) of the MAR were set to zero during initialization. The DMAC 209...

...62 in the format shown in Fig. 45P wherein bits
31-27 = Reserved
26 = High **order** byte count bit. This bit will = 1 only when the maximum byte count is being...

...156 (4096 max). The bus adapter 154 requires a count of 1111 1111 1111 in **order** to transfer 4096 bytes (byte count -1). Therefore, the BCU will decrement the double word...

...offset bits 15-14 (in 64 byte blocks) to bus adapter 154.
15-14 = Low **order** byte count bits. These bits represent the byte offset minus 1 (for bus adapter requirements...

...BSM write select up byte counter 222. Bits 13-07 are stored into the high **order** byte of adapter bus channel 1 A/D register 227. The DMAC responds with a...

...The BSM starting address on the data bus 223 will be captured by the low **order** bytes of the Channel 1 A/D register 227 and BSM write address register 228...

...BCU logic 253 issues a BSM select up command, gating bits "01" into the high **order** bits of command register 225 via bus 290 and places the command and field length...Starting address of local buffer message data in store 210,
15-00 = Reserved.
The high **order** data bus (Bits 31-16) will be loaded into the low **order** (bits 15-0) part of the DMAC channel 3 memory address register

MAR. The high **order** bits (31-16) of MAR were set to zero during initialization. The DMAC 209 responds...

...07 = Customer/IOA space bit
06-00 = Reserved
The DMAC 209 will load the high **order** word (byte count) of the data
...A Read BCU Status Command can be issued by the S/88 processor 62 in **order** to read the current status of the BCU 156. The command is placed on the...

...Power on Reset to the BCU 156. It can be issued at any time in **order** to clear the BCU of any abnormal conditions. However, a local bus cycle (007EXXXX decode...updated appropriately.
When the System/88 is booted, these entries are placed in sequential address **order** in the freelist; only a few pages at this time are assigned for use. Hence...Array of Fig. 47 conceptually illustrates all of the mme arrays arranged in sequential address **order** .
Mme's are usually threaded onto one of three lists:
1.) used list, mme assigned...

...256 MB of real storage. Each of these pointers comprise the 16 most significant (high **order**) bits of a physical address, called a physical page number (ppn), and are used as a pointer to a specific mme. The seven high **order** bits of the ppn select the mme array, and the nine low **order** bits of the ppn select the mme within the array. The twelve low **order** bits of the physical address are an offset into the real (physical) page of storage...a new system and can be modified by the customer to suit his requirements. In **order** to capture a 5/370 area 162-164 from the S/88 main storage 16...

6/3,K/5 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00473016 **Image available**
A CAMERA WITH INTERNAL PRINTING SYSTEM
APPAREIL PHOTOGRAPHIQUE A SYSTEME D'IMPRESSION INTERNE
Patent Applicant/Assignee:
SILVERBROOK RESEARCH PTY LIMITED,
SILVERBROOK Kia,
WALMSLEY Simon,
LAPSTUN Paul,
Inventor(s):
SILVERBROOK Kia,
WALMSLEY Simon,
LAPSTUN Paul,
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19970715; AU 978025 19970715; AU 978032 19970715; AU 977999 19970715;
AU 978024 19970715; AU 978016 19970715; AU 978030 19970715; AU 977938
19970715; AU 977997 19970715; AU 977979 19970715; AU 978015 19970715;
AU 977978 19970715; AU 977982 19970715; AU 977989 19970715; AU 978019
19970715; AU 977980 19970715; AU 977942 19970715; AU 978018 19970715;
AU 978021 19970715; AU 978000 19970715; AU 977940 19970715; AU 977939
19970715; AU 978020 19970715; AU 977985 19970715; AU 977987 19970715;
AU 978022 19970715; AU 978029 19970715; AU 978023 19970715; AU 978028
19970715; AU 978027 19970715; AU 978026 19970715; AU 977983 19970715;
AU 977986 19970715; AU 977981 19970715; AU 977977 19970715; AU 977934
19970715; AU 977990 19970715; AU 978497 19970811; AU 978505 19970811;
AU 978498 19970811; AU 978504 19970811; AU 978501 19970811; AU 978500
19970811; AU 978502 19970811; AU 978499 19970811; AU 979395 19970923;
AU 979404 19970923; AU 979394 19970923; AU 979396 19970923; AU 979397
19970923; AU 979398 19970923; AU 979399 19970923; AU 979400 19970923;
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Detailed Description
... ink is to be deposited, said media and ink supply means including a roll of **media** rolled upon a **media** former within said **media** and ink supply means and at least one ink reservoir integrally formed within said **media** and ink supply means and adapted to be connected to said printing mechanism for the...to the computer systems for printing out corresponding cards by the printer systems.

Preferably the **computer** systems **store** the series of image manipulation card data in a cached manner over the computer network...of 32 bytes in 25ns), it is not efficient dealing with single byte requests.
In **order** to reduce effective mernory latency, the ACP 31 contains 128 cache lines. Each cache line...FIFO 78
A client writes 8-bit data to the VLIW Input FIFO 78 in **order** to have the data processed by the VLIW Vector Processor 74. Clients include the Image...bits
1 1 = 24 bits
4 Which bytes of R to update (hi to lo **order** byte)
Each of the 4 bits represents 1 byte WriteEnable on R
10 TOTAL
write...B are treated as four 8 bit numbers Ao thru A3 (AO is the low **order** byte), and Bo thru B3. Agen, Bgen, and Fgen are responsible for ordering the inputs...write or read & write pixels for their client. Read Iterators read pixels in a specific **order** for their clients, and Write Iterators write pixels in a specifie **order** for their clients. Clients of Iterators read pixels from the local Input FIFO or write...

...via the local Output FIFO.

Read Image Iterators read through an image in a specific **order** , placing the pixel data into the local Input FIFO.
Every time a client reads a...

...the Data cache 76) into the FIFO.

Write Image Iterators write pixels in a specific **order** to write out the entire image. Clients write pixels to the Output FIFO that

is...Address
Generator acts as a Read Iterator, and therefore reads the image in a particular **order** , placing the pixels into the Input FIFO.

When WriteEnable is set, the I/0 Address Generator acts as a Write Iterator, and therefore writes the image in a particular **order** , taking
the pixels from the Output FIFO.

When both ReadEnable and WriteEnable are set, the...perform some process
on each pixel from an imacre but don't care about the **order** of the pixels being processed, or want the data specifically in this **order** . Complementing the Sequential Read Iterator is the Sequential Write Iterator. Clients write pixels to the...

...appropriately.

Box Read Iterator
The Box Read Iterator is used to present pixels in an **order** most useful
for performing operations such as generalpurpose filters and convolve. The Iterator presents pixel...Write Iterators
In some instances it is necessary to write an image in output pixel **order** , but there is no knowledge about the direction of coherence in input pixels in relation...

...the input pixels (such as color coherence), in which case the read governs the processing **order** , and the write, to be synchronized, must
follow the same pixel **order** .

The **order** of pixels presented as input (Vertical-Strip Read), or expected for output (Vertical-Strip Write) is the same.

The **order** is pixels 0 to 31 from line 0, then pixels 0 to 31 of fine...
table. Given fixed-point X and Y coordinates (placed into the Output FIFO
in the **order** Y, X), 4 values are returned after lookup. The values (in
order) are.

Table[Int(X), Int(Y)]
Table[Int(X)+1, Int(Y)]
Table[Int(X), Int(Y)+1]
Table[Int(X)+1, Int(Y)+1]
The **order** of values retur-ned gives the best cache coherence. 1f the data is 8-bit, 2 values are returned each cycle over 2 cycles with the low **order** byte being the first data element. 1f the data is 16-bit, the
4 values...12bit ZOffset register. In this form of lookup, given 3 fixed-point indexes in the **order** Z, Y, X, 8 values are returned in **order** from the lookup table.

-7 0
Table[Int(X), Int(Y), Int(Z)]

Table[Int...

...I, Int(Z)+1]
Table[Int(X)+1, Int(Y)+I, Int(Z)+1]
The **order** of values returned gives the best cache coherence. If the data is 8-bit, 2 values are returned each cycle over 4 cycles with the low **order** byte being the first data element. lf the data is 16-bit, the
4 values...multi-cycle generation.

Generate Sequential [X, Yl
When a process is processincr pixels in sequential **order** according to
the Sequential Read Iterator (or generating pixels and writing them out
to a...

...2 0 0
Generate Vertical Strip [X, YI
When a process is processing pixels in **order** to write them to a Vertical Strip Write Iterator, and for some reason cannot use...

...control information to the Image Sensor, including frame sync pulses and
pixel clock pulses in **order** to read the image.

Pixels are read from the image sensor and placed into the...using the accelerated Vark Affine Transform function. The processing is performed
in 2 steps in **order** to reduce design complexity and to re-use the Vark
affine transform rotate logic already...

...orientation.. The processed imaue may also have to be rotated during the
Print process in **order** to be in the correct orientation for printing.
The 3D mode] of the Artcam has...etc.

Pixels are stored in an interleaved fashion since all color components
are required in **order** to convert to the internal image format.
It should be noted that the ACP 31...ImaPound Sterling!e Organizatio
The entire processed imaore is required at the same time in **order** to print it. However the Print Image output can comprise a CMY dithered image and...that sends control information to the linear sensor, including LineSync pulses and PixelClock pulses in **order** to read the image. Pixels are read from the linear sensor and placed into the...The
top 3 elements in the FIFO 247 can be accessed 252 in any random **order** .
The run lengths (in pixels) of these entries are filtered into 3 values:
short, mediunz...468,255ns or 0.015 seconds.

Step 0: Advance to the next dot column
In **order** to advance to the next column of dots we add Arow and

Acolumn
to the...

...whole column.

Ste12 1: Detect the to12 and bottom of an Artcard dot column.

In **order** to process a dot column from an Artcard, it is necessary to detect the top...uses the distance of the centroid from the center of the middle pixel 291 in **order** to select 3 representative pixels and thus decide the value of the dot.
Pixel 1...not need updatincr. Otherwise a process of chancring the centroid As needs to occur in **order** to best fit the expected centroid location to the actual data. The new centroid As...2 sets of 2MB areas are utilised. The scrambled data 331 is in symbol block **order** arrancred in a 16x 16 array, with symbol block 0 (334) having all the symbol O's from all the code words in random **order** . Symbol block 1 has all the symbol l's from all the code WO 99...printed at a particular pitch (eor. 1600 dpi), the dots themselves are slightly larger in **Order** to create continuous lines when dots are printed contiguously. In the example images of Fig...

...ink/printing behaviour for a particular printing technology should be studied in more detail in **order** to obtain best results.

In describing this artcard embodiment, the term dot refers to a... right-to-left.

Regardless of reading direction, the orientation does need to be deterinined in **order** to extract the data from the data region.

Orientation columns
As illustrated in Fig. 56 reverse the process in **order** to extract the original data from the dots on an alternative Artcard.

At first glance...

...that each Reed-Solomon encoded block size n is 255 bytes (2 8 ,symbols). In **order** to allow correction of up to t symbols, 2t symbols in the final block size...block has a StartPixel and an EndPixel to deternUne where to loOk for targets in **order** to locate the data block's data region.

lf the pixel value is in the...or
NotATarget
Processing Targets
he located targets (in the LocatedTargets list) are stored in the **order**

they were located. Depending on alternative Artcard rotation these targets will be in ascending pixel **order** or descending pixel **order**

In addition, the target numbers recovered from the targets may be in error. We may...

...target number due to dirt). Two main steps are involved.
Sort targets into ascending pixel **order**
Locate and fix erroneous target numbers
The first step is simple. The nature of the...of the target. It is possible to assume that ascending targets have pixels in ascending **order**
(since they have already been sorted).

kPixelFactor = 1/(55 * 3)
bestTarget = 0
bestChanges = TargetsFound + 1...to X, and 6 points for X to X+I, requiring 7 points overall in **order** to get pixel values from X- 1 to X+
1 since some of the pixels...data dot (CurrentDot), and the delta amounts to be added to that center position in **order** to advance to subsequent dots in the coluinn (DataDelta).

The first thing to do is...preferred embodirnent has the ability to use the surrounding dots in the same column in **order** to make a better decision about a dot's value. Since the previous column's...is a lookup table in DRAM. The kemel is arranged with coefficients in the same **order** as the Box Read Iterator 342. Each coefficient entry is 8 bits. A simple Sequential...so as to map the theoretical image to the corresponding actual input image 367.
In **order** to deternUne the actual value and output image pixel should take so as to avoid...

...is utilised as will become more apparent hereinafter.

The image warper performs several tasks in **order** to warp an image.

Scale the warp map to match the output image size.

Determine...approximation of the actual shape.

Preferably, the points are processed in a vertical strip output **order**,
PO is the previous point on the same line within a strip, and when PI...
that output pixels are written in a vertical strip (via a Vertical-Strip Iterator) in **order** to best make use of cache coherence.

Tri-linear interpolation can be completed in as...The 8-bit input color

components are treated as fixed-point numbers (3:5) in **order** to index
into the conversion tables. The 3 bits of integer give the index, and...
by a slightly altered version of Fant's resampling algorithrn to account
for processing in **order** of X pixels.
Where the following constants are set by software.

Constant Value
K, Number...

Claim
... method as claimed in clairn 305 wherein said predetermined areas are
selected in a predetermined **order** . 307. A method as claimed in claim
305 wherein said printing utilizes a high resolution...
?